What is claimed is:

1. An integrated circuit structure comprising:

a plastic substrate;

a layer of silicon dioxide or silicon nitride having a thickness such that little or no differential strain between the substrate and said layer occurs in the normal operating temperature range of said integrated circuit;

an antenna conductor which is bonded onto, integrated onto or printed onto said substrate and having two conductive pads or other conductive terminal areas where electrical connection to said antenna may be made;

an RFID tag or smart card transceiver integrated circuit integrated on said substrate so as to have RF input/output terminals which are electrically coupled to said terminal areas of said antenna.

2. An integrated circuit structure comprising:

a plastic substrate;

a layer of silicon dioxide or silicon nitride having a thickness such that little or no differential strain between the substrate and said layer occurs in the normal operating temperature range of said integrated circuit;

an RFID tag or smart card transceiver integrated circuit integrated on said substrate on top of said layer of silicon dioxide or silicon nitride so as to have RF input/output terminals, and having a layer of insulating material formed over said integrated circuit;

an antenna conductor which is bonded onto, integrated onto or printed onto said insulating layer covering said integrated circuit so as to make electrical connection with said RF input/output terminals.

3. An integrated circuit structure comprising:

a first plastic or glass or plastic laminated to glass substrate;

a layer of silicon dioxide or silicon nitride having a thickness such that little or no differential strain between the substrate and said layer occurs in the normal operating temperature range of said integrated circuit;

an antenna conductor which is bonded onto, integrated onto or printed onto said substrate and having two conductive pads or other conductive terminal areas where electrical connection to said antenna may be made;

an RFID tag or smart card transceiver integrated circuit integrated as one of a very large number of said integrated circuits on a large second plastic or glass substrate using flat panel display manufacturing equipment, said integrated circuit being cut from said second plastic or glass substrate and bonded or otherwised attached to said first plastic substrate and having RF input/output terminals; and

wires connected in any way between said RF input/output terminals of said integrated circuit and said terminal areas of said antenna.

4. A process of making a large number of integrated circuits on a large plastic or glass or plastic laminated to glass substrate comprising:

selecting a plastic or glass or plastic laminated to glass substrate having a large size which is compatible with the substrate size capacity of flat panel display manufacturing machines to be used to do the subsequent deposition, photolithography, etching and laser crystallization and annealing steps necessary to form an integrated circuit thereon;

depositing a layer of insulating material which has a thickness and Young's Modulus which are selected in light of the thickness and Young's Modulus of said substrate so as to reduce differential strain at anticipated operating temperatures so as to eliminate or reduce reliability problems using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals which will not chemically attack or otherwise damage said substrate;

forming an antenna with one or more terminals on said layer of insulating material using processing steps performed at temperatures or in a manner which

will not exceed the glass transition temperature of said substrate and using chemicals which will not chemically attack or otherwise damage said substrate;

using flat panel display manufacturing machines to deposit a layer of insulating material over said antenna and to do the insulation, metal and semiconductor deposition steps, and the photolighography, etching and pulsed laser crystallization and annealing steps necessary to form an integrated circuit of a desired functionality directly on said substrate so as to RF input/output terminals in electrical contact with said one or more antenna terminals, all said processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals which will not chemically attack or otherwise damage said substrate.

5. A process of making a large number of integrated circuits on a large substrate comprising:

selecting a first plastic or glass or plastic laminated to glass substrate having a large size which is compatible with the substrate size capacity of flat panel display manufacturing machines to be used to do the subsequent deposition, photolithography, etching steps needed to form an antenna or compatible with the substrate size capacity that can be processed by a silk screen printer to print an antenna;

depositing a layer of insulating material which has a thickness and Young's Modulus which are selected in light of the thickness and Young's Modulus of said substrate so as to reduce differential strain at anticipated operating temperatures so as to eliminate or reduce reliability problems using a process which will not melt, warp, deform, chemically attack or otherwise damage said first substrate;

using a flat panel display manufacturing machine or silk screen printer to form a plurality of antennas at a plurality of locations on said first substrate with one or more terminals on said layer of insulating material using deposition, photolithography, etching or printing processes which will not melt, warp, deform, chemically attack or otherwise damage said first substrate;

dicing said first substrate up into many individual substrates, each with its own antenna formed thereon;

selecting a second plastic or glass or plastic laminated to glass substrate having a large size which is compatible with the substrate size capacity of flat panel display manufacturing machines to be used to do subsequent deposition, photolithography, etching and laser crystallization and annealing steps necessary to form a thin film integrated circuit;

using flat panel display manufacturing machines to do the insulation, metal and semiconductor deposition steps, and the photolighography, etching and pulsed laser crystallization and annealing steps necessary to form an integrated circuit of a desired functionality on said second substrate so as to RF input/output terminals, all said processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said second substrate and using chemicals which will not chemically attack or otherwise damage said second substrate;

dicing said second substrate up into many integrated circuits and bonding or otherwise attaching each functional integrated circuit to one of said individual plastic substrates cut from said first substrate; and

wire bonding wires to connect said RF input/output terminals of said integrated circuit to said one or more terminals of said antenna on said individual first substrate.

6. A process of making a large number of integrated EEPROM cells on a large substrate comprising:

selecting a plastic or plastic laminated to glass substrate having a large size which is compatible with the substrate size capacity of flat panel display manufacturing machines to be used to do the subsequent deposition, photolithography, etching and laser crystallization and annealing steps necessary to form said EEPROM cells thereon;

depositing a layer of insulating material which has a thickness and Young's Modulus which are selected in light of the thickness and Young's Modulus of said substrate so as to reduce differential strain at anticipated operating temperatures so as to eliminate or reduce reliability problems using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature

of said plastic substrate and using chemicals which will not chemically attack or otherwise damage said plastic substrate;

using flat panel display manufacturing machines to do the insulation, metal and semiconductor deposition steps, and the photolighography, etching and pulsed laser crystallization and annealing steps necessary to form a plurality of EEPROM memory cells directly on said plastic substrate, all said processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said plastic substrate and using chemicals which will not chemically attack or otherwise damage said plastic substrate.

7. A process for manufacturing an integrated circuit including MOS transistors and EEPROM cells on a substrate comprising:

selecting a plastic or plastic laminated to glass substrate having a large size which is compatible with the substrate size capacity of flat panel display manufacturing machines to be used to do the subsequent deposition, photolithography, etching and laser crystallization and annealing steps necessary to form said integrated circuit thereon;

using flat panel display manufacturing machines to perform the following steps:

depositing a layer of insulating material which has a thickness and Young's Modulus which are selected in light of the thickness and Young's Modulus of said substrate so as to reduce differential strain at anticipated operating temperatures so as to eliminate or reduce reliability problems using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals which will not chemically attack or otherwise damage said substrate;

depositing a layer of amorphous silicon which is between 10 and 5000 nanometers thick by sputtering or by plasma enhanced chemical vapor deposition hereafter referred to as PECVD using processing steps performed at temperatures or in a manner which will not exceed the glass transition

temperature of said substrate and using chemicals and/or gases which will not chemically attack or otherwise damage said substrate;

if higher mobilities or higher ON currents or lower threshold voltages for MOS transistors are needed for the transistors to be formed in said silcon layer than can be achieved in amorphous silicon, crystallizing said silicon layer to polycrystalline or microcrystalline form by pulse annealing the silcon layer with an excimer laser having a 308 nm wavelength using pulse durations of 30 nanoseconds or less full width at half maximum and energy density between 30-600 mJ/cm^2 per pulse using one or more pulses;

masking off areas of said integrated circuit where EEPROM cells, if any, are to be formed, and depositing a layer of gate insulator by PECVD at a temperature below the glass transistion temperature of said substrate, said layer having a thickness suitable for thin film metal-oxide-semiconductor transistor device operation, typically between 20-500 nanometers thick;

masking off areas where MOS transistors are being formed to expose areas where EEPROM memory cells are to be formed and depositing one or more layers of gate insulator to form an insulation layer that is to lie below the floating gate, the thickness and materials selected for said one or more layers of gate insulator being such as to achieve Fowler-Noordheim tunnelling to the floating gate from a channel region at whatever programming voltage can be achieved on said integrated circuit, said deposition being accomplished by PECVD at a temperature below the glass transition temperature of said substrate;

depositing a layer of gate conductor, typically metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process to form a control gate at the MOS transistor locations and a floating gate at the EEPROM cell locations, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where EEPROM cells are being formed, and depositing a

layer of intergate insulator from which will be formed the insulation layer between the floating gate and the control gate of each EEPROM cell, said deposition being accomplished by PECVD or some other process which will form an insulator of high enough quality to prevent charge leakage from said floating gate and at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where EEPROM cells are being formed, and depositing a layer of metal or silicide from which the control gate of all EEPROM cells is to be formed, said deposition being by PVD, CVD, PECVD, evaporation or sputtering or some other suitable process and accomplished at a temperature below the glass transition temperature of said substrate;

performing the necessary photolithographic etching to define the gate islands at both said MOS transistor and EEPROM cell locations, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

doping the source and drain regions of all said MOS transistors and EEPROM cells using the Gas Immersion Laser Doping process or any other suitable doping process which can dope said source and drain regions to suitable conductivity and which crystallizes said amorphous silicon by pulsed laser annealing and which can be accomplished at a temperature below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

photolithographically etching to define the lateral extents of each thin film transistor island at each MOS transistor and EEPROM cell, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

depositing an insulation layer over all MOS transistors and EEPROM cells and etching vias therethrough for source, drain and control gate contacts

at all MOS transistor and EEPROM cell locations, said deposition being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing a layer of contact metallization conductor to fill said via holes and cover each MOS transistors and EEPROM cell location and the spaces therebetween, and photolithographically etching the conductor layer to form a contact metallization to connect all the MOS transistors and EEPROM cells together to form the desired integrated circuit functionality.

8. The process of claim 7 wherein said integrated circuit is an RFID tag transceiver, a smart card or a toy controller and further comprising the steps of etching said contact metallization conductor layer appropriately to form RF input/output terminals, and further comprising the step of printing or photolithographically forming a conductive antenna on said substrate so as to make electrical contact with said RF input/output terminals.

9. A process for manufacturing an integrated circuit including MOS transistors and ROM cells on a substrate comprising:

selecting a plastic or plastic laminated to glass substrate having a large size which is compatible with the substrate size capacity of flat panel display manufacturing machines to be used to do the subsequent deposition, photolithography, etching and laser crystallization and annealing steps necessary to form said integrated circuit thereon;

using flat panel display manufacturing machines to perform the following steps:

depositing a layer of insulating material which has a thickness and Young's Modulus which are selected in light of the thickness and Young's Modulus of said substrate so as to reduce differential strain at anticipated operating temperatures so as to eliminate or reduce reliability problems using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using

chemicals which will not chemically attack or otherwise damage said substrate;

depositing a layer of amorphous silicon which is between 10 and 500 nanometers thick by sputtering or by plasma enhanced chemical vapor deposition hereafter referred to as PECVD using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals and/or gases which will not chemically attack or otherwise damage said substrate;

if higher mobilities or higher ON currents or lower threshold voltages for MOS transistors are needed for the transistors to be formed in said silcon layer than can be achieved in amorphous silicon, crystallizing said silicon layer to polycrystalline or microcrystalline form by pulse annealing the silcon layer with an excimer laser having a 308 nm wavelength using pulse durations of 30 nanoseconds or less full width at half maximum and energy density between 30-600 mJ/cm^2 per pulse using one or more pulses;

masking off areas of said integrated circuit where ROM cells, if any, are to be formed, and depositing a layer of gate insulator by PECVD at a temperature below the glass transistion temperature of said substrate, said layer having a thickness suitable for thin film metal-oxide-semiconductor transistor device operation, typically between 20-500 nanometers thick;

masking off areas where MOS transistors are being formed to expose areas where ROM memory cells are to be formed and depositing one or more layers of gate insulator to form an insulation layer that is to lie below the floating gate, the thickness and materials selected for said one or more layers of gate insulator being such as to achieve Fowler-Noordheim tunnelling to the floating gate from a channel region at whatever programming voltage can be achieved on said integrated circuit, said deposition being accomplished by PECVD at a temperature below the glass transition temperature of said substrate;

depositing a layer of gate conductor, typically metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition

(hereafter CVD), PECVD, evaporation or sputtering or some other suitable process to form a control gate at the MOS transistor locations and a floating gate at the ROM cell locations, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where ROM cells are being formed, and depositing a layer of intergate insulator from which will be formed the insulation layer between the floating gate and the control gate of each ROM cell, said deposition being accomplished by PECVD or some other process which will form an insulator of high enough quality to prevent charge leakage from said floating gate and at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where ROM cells are being formed, and depositing a layer of metal or silicide from which the control gate of all ROM cells is to be formed, said deposition being by PVD, CVD, PECVD, evaporation or sputtering or some other suitable process and accomplished at a temperature below the glass transition temperature of said substrate;

performing the necessary photolithographic etching to define the gate islands at both said MOS transistor and ROM cell locations, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

doping the source and drain regions of all said MOS transistors and ROM cells using the Gas Immersion Laser Doping process or any other suitable doping process which can dope said source and drain regions to suitable conductivity and which crystallizes said amorphous silicon by pulsed laser annealing and which can be accomplished at a temperature below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

photolithographically etching to define the lateral extents of each thin film transistor island at each MOS transistor and ROM cell, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

depositing an insulation layer over all MOS transistors and ROM cells and etching vias therethrough for source, drain and control gate contacts at all MOS transistor and ROM cell locations, said deposition being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing a layer of contact metallization conductor to fill said via holes and cover each MOS transistors and ROM cell location and the spaces therebetween, and photolithographically etching the conductor layer to form a contact metallization to connect all the MOS transistors and ROM cells together to form the desired integrated circuit functionality.

10. A process for manufacturing an integrated circuit with MOS and EEPROM cells formed over an antenna on a substrate comprising:

selecting a plastic or plastic laminated to glass substrate having a large size which is compatible with the substrate size capacity of flat panel display manufacturing machines to be used to do the subsequent deposition, photolithography, etching and laser crystallization and annealing steps necessary to form said integrated circuit thereon;

using flat panel display manufacturing machines to perform the following steps:

depositing a layer of insulating material which has a thickness and Young's Modulus which are selected in light of the thickness and Young's Modulus of said substrate so as to reduce differential strain at anticipated operating temperatures so as to eliminate or reduce reliability problems using processing steps performed at temperatures or in a manner which will

not exceed the glass transition temperature of said substrate and using chemicals which will not chemically attack or otherwise damage said substrate;

forming an antenna with one or more terminals on said layer of insulating material deposited in the previous step at a plurality of locations on said substrate by any prior art process such as silk screening or deposition and photolithographic etching accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases that will not attack or otherwise damage said substrate;

using flat panel display manufacturing machines to perform the following steps:

depositing a layer of pad contact conductor such as metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process and photolithographically etching to form lead line conductors from each antenna terminal to the locations where RF input/output terminals of each corresponding integrated circuit will be formed, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

depositing a layer of insulator over all MOS transistor and EEPROM cell locations and etching to form vias through said insulation layer where source and drain contacts are to be formed, said deposition being accomplished by PECVD or some other process which will form an insulator of high enough quality and at a temperature below the glass transition temperature of said substrate using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing a layer of contact metallization conductor such as metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process and photolithographically etching to form lead line

conductors to make all necessary source and drain connections from each MOS transistor or EEPROM cell to other devices needed to establish at least part of the connections needed for the functionality of the integrated circuit being formed, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

depositing a layer of amorphous silicon which is between 10 and 5000 nanometers thick by sputtering or by plasma enhanced chemical vapor deposition hereafter referred to as PECVD using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals and/or gases which will not chemically attack or otherwise damage said substrate;

if higher mobilities or higher ON currents or lower threshold voltages for MOS transistors are needed for the transistors to be formed in said silcon layer than can be achieved in amorphous silicon, crystallizing said silicon layer to polycrystalline or microcrystalline form by pulse annealing the silcon layer with an excimer laser having a 308 nm wavelength using pulse durations of 30 nanoseconds or less full width at half maximum and energy density between 30-600 mJ/cm^2 per pulse using one or more pulses;

masking off areas of said integrated circuit where EEPROM cells, if any, are to be formed, and depositing a layer of gate insulator by PECVD at a temperature below the glass transistion temperature of said substrate, said layer having a thickness suitable for thin film metal-oxide-semiconductor transistor device operation, typically between 20-500 nanometers thick;

masking off areas where MOS transistors are being formed to expose areas where EEPROM memory cells are to be formed and depositing one or more layers of gate insulator to form an insulation layer that is to lie below the floating gate, the thickness and materials selected for said one or more layers of gate insulator being such as to achieve Fowler-Noordheim tunnelling to the floating gate from a channel region at whatever programming voltage can be achieved on said integrated circuit, said

deposition being accomplished by PECVD at a temperature below the glass transition temperature of said substrate;

depositing a layer of gate conductor, typically metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process to form a control gate at the MOS transistor locations and a floating gate at the EEPROM cell locations, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where EEPROM cells are being formed, and depositing a layer of intergate insulator from which will be formed the insulation layer between the floating gate and the control gate of each EEPROM cell, said deposition being accomplished by PECVD or some other process which will form an insulator of high enough quality to prevent charge leakage from said floating gate and at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where EEPROM cells are being formed, and depositing a layer of metal or silicide from which the control gate of all EEPROM cells is to be formed, said deposition being by PVD, CVD, PECVD, evaporation or sputtering or some other suitable process and accomplished at a temperature below the glass transition temperature of said substrate;

performing the necessary photolithographic etching to define the gate islands at both said MOS transistor and EEPROM cell locations, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

doping the source and drain regions of all said MOS transistors and EEPROM cells using the Gas Immersion Laser Doping process or any other suitable doping process which can dope said source and drain regions to suitable conductivity and which crystallizes said amorphous silicon by pulsed

laser annealing and which can be accomplished at a temperature below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

photolithographically etching to define the lateral extents of each thin film transistor island at each MOS transistor and EEPROM cell, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

depositing an insulation layer over all MOS transistors and EEPROM cells and etching vias therethrough for control gate contacts at all MOS transistor and EEPROM cell locations, said deposition being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing a layer of contact metallization conductor to fill said via holes and cover each MOS transistors and EEPROM cell location and the spaces therebetween, and photolithographically etching the conductor layer to form a contact metallization to connect all the control gates of all MOS transistors and EEPROM cells to other nodes in the circuit to form the rest of the connections necessary to form a desired integrated circuit functionality.

11. A process for manufacturing an integrated circuit with MOS and ROM cells formed over an antenna on a substrate comprising:

selecting a plastic or plastic laminated to glass substrate having a large size which is compatible with the substrate size capacity of flat panel display manufacturing machines to be used to do the subsequent deposition, photolithography, etching and laser crystallization and annealing steps necessary to form said integrated circuit thereon;

using flat panel display manufacturing machines to perform the following steps:

depositing a layer of insulating material which has a thickness and Young's Modulus which are selected in light of the thickness and Young's Modulus of said substrate so as to reduce differential strain at anticipated operating temperatures so as to eliminate or reduce reliability problems using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals which will not chemically attack or otherwise damage said substrate;

forming an antenna with one or more terminals on said layer of insulating material deposited in the previous step at a plurality of locations on said substrate by any prior art process such as silk screening or deposition and photolithographic etching accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases that will not attack or otherwise damage said substrate;

using flat panel display manufacturing machines to perform the following steps:

depositing a layer of pad contact conductor such as metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process and photolithographically etching to form lead line conductors from each antenna terminal to the locations where RF input/output terminals of each corresponding integrated circuit will be formed, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

depositing a layer of insulator over all MOS transistor and ROM cell locations and etching to form vias through said insulation layer where source and drain contacts are to be formed, said deposition being accomplished by PECVD or some other process which will form an insulator of high enough quality and at a temperature below the glass transition temperature of said

substrate using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing a layer of contact metallization conductor such as metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process and photolithographically etching to form lead line conductors to make all necessary source and drain connections from each MOS transistor or ROM cell to other devices needed to establish at least part of the connections needed for the functionality of the integrated circuit being formed, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

depositing a layer of amorphous silicon which is between 10 and 5000 nanometers thick by sputtering or by plasma enhanced chemical vapor deposition hereafter referred to as PECVD using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals and/or gases which will not chemically attack or otherwise damage said substrate;

if higher mobilities or higher ON currents or lower threshold voltages for MOS transistors are needed for the transistors to be formed in said silcon layer than can be achieved in amorphous silicon, crystallizing said silicon layer to polycrystalline or microcrystalline form by pulse annealing the silcon layer with an excimer laser having a 308 nm wavelength using pulse durations of 30 nanoseconds or less full width at half maximum and energy density between 30-600 mJ/cm^2 per pulse using one or more pulses;

masking off areas of said integrated circuit where ROM cells, if any, are to be formed, and depositing a layer of gate insulator by PECVD at a temperature below the glass transistion temperature of said substrate, said layer having a thickness suitable for thin film metal-oxide-semiconductor transistor device operation, typically between 20-500 nanometers thick;

masking off areas where MOS transistors are being formed to expose areas where ROM memory cells are to be formed and depositing one or more

layers of gate insulator to form an insulation layer that is to lie below the floating gate, the thickness and materials selected for said one or more layers of gate insulator being such as to achieve Fowler-Noordheim tunnelling to the floating gate from a channel region at whatever programming voltage can be achieved on said integrated circuit, said deposition being accomplished by PECVD at a temperature below the glass transition temperature of said substrate;

depositing a layer of gate conductor, typically metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process to form a control gate at the MOS transistor locations and a floating gate at the ROM cell locations, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where ROM cells are being formed, and depositing a layer of intergate insulator from which will be formed the insulation layer between the floating gate and the control gate of each ROM cell, said deposition being accomplished by PECVD or some other process which will form an insulator of high enough quality to prevent charge leakage from said floating gate and at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where ROM cells are being formed, and depositing a layer of metal or silicide from which the control gate of all ROM cells is to be formed, said deposition being by PVD, CVD, PECVD, evaporation or sputtering or some other suitable process and accomplished at a temperature below the glass transition temperature of said substrate;

performing the necessary photolithographic etching to define the gate islands at both said MOS transistor and ROM cell locations, said photolithographic etching being accomplished at temperatures below the glass

transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

doping the source and drain regions of all said MOS transistors and ROM cells using the Gas Immersion Laser Doping process or any other suitable doping process which can dope said source and drain regions to suitable conductivity and which crystallizes said amorphous silicon by pulsed laser annealing and which can be accomplished at a temperature below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

photolithographically etching to define the lateral extents of each thin film transistor island at each MOS transistor and ROM cell, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

depositing an insulation layer over all MOS transistors and ROM cells and etching vias therethrough for control gate contacts at all MOS transistor and ROM cell locations, said deposition being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing a layer of contact metallization conductor to fill said via holes and cover each MOS transistors and ROM cell location and the spaces therebetween, and photolithographically etching the conductor layer to form a contact metallization to connect all the control gates of all MOS transistors and ROM cells to other nodes in the circuit to form the rest of the connections necessary to form a desired integrated circuit functionality.

12. A process of making a large number of integrated EEPROM or ROM or static RAM cells on a large substrate comprising:

selecting a glass substrate having a large size which is compatible with the substrate size capacity of flat panel display manufacturing machines to be used to do

the subsequent deposition, photolithography, etching and laser crystallization and annealing steps necessary to form said EEPROM or ROM or static RAM cells thereon;

using flat panel display manufacturing machines to do the insulation, metal and semiconductor deposition steps, and the photolighography, etching and pulsed laser crystallization and annealing steps necessary to form a plurality of EEPROM or ROM or static RAM memory cells directly on said glass substrate, all said processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals which will not chemically attack or otherwise damage said substrate.

13. A process for manufacturing an integrated circuit including MOS transistors and EEPROM cells on a substrate comprising:

selecting a glass substrate having a large size which is compatible with the substrate size capacity of flat panel display manufacturing machines to be used to do the subsequent deposition, photolithography, etching and laser crystallization and annealing steps necessary to form said integrated circuit thereon;

using flat panel display manufacturing machines to perform the following steps:

depositing a layer of insulating material using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals which will not chemically attack or otherwise damage said substrate;

depositing a layer of amorphous silicon which is between 10 and 5000 nanometers thick by sputtering or by plasma enhanced chemical vapor deposition hereafter referred to as PECVD using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals and/or gases which will not chemically attack or otherwise damage said substrate;

if higher mobilities or higher ON currents or lower threshold voltages for MOS transistors are needed for the transistors to be formed in said silcon layer than can be achieved in amorphous silicon, crystallizing said

silicon layer to polycrystalline or microcrystalline form by pulse annealing the silcon layer with an excimer laser having a 308 nm wavelength using pulse durations of 30 nanoseconds or less full width at half maximum and energy density between 30-600 mJ/cm^2 per pulse using one or more pulses;

masking off areas of said integrated circuit where EEPROM cells, if any, are to be formed, and depositing a layer of gate insulator by PECVD at a temperature below the glass transistion temperature of said substrate, said layer having a thickness suitable for thin film metal-oxide-semiconductor transistor device operation, typically between 20-500 nanometers thick;

masking off areas where MOS transistors are being formed to expose areas where EEPROM memory cells are to be formed and depositing one or more layers of gate insulator to form an insulation layer that is to lie below the floating gate, the thickness and materials selected for said one or more layers of gate insulator being such as to achieve Fowler-Noordheim tunnelling to the floating gate from a channel region at whatever programming voltage can be achieved on said integrated circuit, said deposition being accomplished by PECVD at a temperature below the glass transition temperature of said substrate;

depositing a layer of gate conductor, typically metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process to form a control gate at the MOS transistor locations and a floating gate at the EEPROM cell locations, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where EEPROM cells are being formed, and depositing a layer of intergate insulator from which will be formed the insulation layer between the floating gate and the control gate of each EEPROM cell, said deposition being accomplished by PECVD or some other process which will form an insulator of high enough quality to prevent charge leakage from said

floating gate and at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where EEPROM cells are being formed, and depositing a layer of metal or silicide from which the control gate of all EEPROM cells is to be formed, said deposition being by PVD, CVD, PECVD, evaporation or sputtering or some other suitable process and accomplished at a temperature below the glass transition temperature of said substrate;

performing the necessary photolithographic etching to define the gate islands at both said MOS transistor and EEPROM cell locations, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

doping the source and drain regions of all said MOS transistors and EEPROM cells using the Gas Immersion Laser Doping process or any other suitable doping process which can dope said source and drain regions to suitable conductivity and which crystallizes said amorphous silicon by pulsed laser annealing and which can be accomplished at a temperature below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

photolithographically etching to define the lateral extents of each thin film transistor island at each MOS transistor and EEPROM cell, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

depositing an insulation layer over all MOS transistors and EEPROM cells and etching vias therethrough for source, drain and control gate contacts at all MOS transistor and EEPROM cell locations, said deposition being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing a layer of contact metallization conductor to fill said via holes and cover each MOS transistors and EEPROM cell location and the spaces therebetween, and photolithographically etching the conductor layer to form a contact metallization to connect all the MOS transistors and EEPROM cells together to form the desired integrated circuit functionality.

14. A process for manufacturing an integrated circuit including MOS transistors and ROM cells on a substrate comprising:

selecting a glass substrate having a large size which is compatible with the substrate size capacity of flat panel display manufacturing machines to be used to do the subsequent deposition, photolithography, etching and laser crystallization and annealing steps necessary to form said integrated circuit thereon;

using flat panel display manufacturing machines to perform the following steps:

depositing a layer of insulating material using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals which will not chemically attack or otherwise damage said substrate;

depositing a layer of amorphous silicon which is between 10 and 500 nanometers thick by sputtering or by plasma enhanced chemical vapor deposition hereafter referred to as PECVD using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals and/or gases which will not chemically attack or otherwise damage said substrate;

if higher mobilities or higher ON currents or lower threshold voltages for MOS transistors are needed for the transistors to be formed in said silcon layer than can be achieved in amorphous silicon, crystallizing said silicon layer to polycrystalline or microcrystalline form by pulse annealing the silcon layer with an excimer laser having a 308 nm wavelength using pulse durations of 30 nanoseconds or less full width at half maximum and energy density between 30-600 mJ/cm^2 per pulse using one or more pulses;

masking off areas of said integrated circuit where ROM cells, if any, are to be formed, and depositing a layer of gate insulator by PECVD at a temperature below the glass transistion temperature of said substrate, said layer having a thickness suitable for thin film metal-oxide-semiconductor transistor device operation, typically between 20-500 nanometers thick;

masking off areas where MOS transistors are being formed to expose areas where ROM memory cells are to be formed and depositing one or more layers of gate insulator to form an insulation layer that is to lie below the floating gate, the thickness and materials selected for said one or more layers of gate insulator being such as to achieve Fowler-Noordheim tunnelling to the floating gate from a channel region at whatever programming voltage can be achieved on said integrated circuit, said deposition being accomplished by PECVD at a temperature below the glass transition temperature of said substrate;

depositing a layer of gate conductor, typically metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process to form a control gate at the MOS transistor locations and a floating gate at the ROM cell locations, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where ROM cells are being formed, and depositing a layer of intergate insulator from which will be formed the insulation layer between the floating gate and the control gate of each ROM cell, said deposition being accomplished by PECVD or some other process which will form an insulator of high enough quality to prevent charge leakage from said floating gate and at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where ROM cells are being formed, and depositing a layer of metal or silicide from which the control gate of all ROM cells is to be

formed, said deposition being by PVD, CVD, PECVD, evaporation or sputtering or some other suitable process and accomplished at a temperature below the glass transition temperature of said substrate;

performing the necessary photolithographic etching to define the gate islands at both said MOS transistor and ROM cell locations, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

doping the source and drain regions of all said MOS transistors and ROM cells using the Gas Immersion Laser Doping process or any other suitable doping process which can dope said source and drain regions to suitable conductivity and which crystallizes said amorphous silicon by pulsed laser annealing and which can be accomplished at a temperature below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

photolithographically etching to define the lateral extents of each thin film transistor island at each MOS transistor and ROM cell, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

depositing an insulation layer over all MOS transistors and ROM cells and etching vias therethrough for source, drain and control gate contacts at all MOS transistor and ROM cell locations, said deposition being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing a layer of contact metallization conductor to fill said via holes and cover each MOS transistors and ROM cell location and the spaces therebetween, and photolithographically etching the conductor layer to form a contact metallization to connect all the MOS transistors and ROM cells together to form the desired integrated circuit functionality.

15. A process for manufacturing an integrated circuit with MOS and EEPROM cells formed over an antenna on a substrate comprising:

selecting a glass substrate having a large size which is compatible with the substrate size capacity of flat panel display manufacturing machines to be used to do the subsequent deposition, photolithography, etching and laser crystallization and annealing steps necessary to form said integrated circuit thereon;

using flat panel display manufacturing machines to perform the following steps:

depositing a layer of insulating material using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals which will not chemically attack or otherwise damage said substrate;

forming an antenna with one or more terminals on said layer of insulating material deposited in the previous step at a plurality of locations on said substrate by any prior art process such as silk screening or deposition and photolithographic etching accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases that will not attack or otherwise damage said substrate;

using flat panel display manufacturing machines to perform the following steps:

depositing a layer of pad contact conductor such as metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process and photolithographically etching to form lead line conductors from each antenna terminal to the locations where RF input/output terminals of each corresponding integrated circuit will be formed, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

depositing a layer of insulator over all MOS transistor and EEPROM cell locations and etching to form vias through said insulation layer where source and drain contacts are to be formed, said deposition being accomplished by PECVD or some other process which will form an insulator of high enough quality and at a temperature below the glass transition temperature of said substrate using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing a layer of contact metallization conductor such as metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process and photolithographically etching to form lead line conductors to make all necessary source and drain connections from each MOS transistor or EEPROM cell to other devices needed to establish at least part of the connections needed for the functionality of the integrated circuit being formed, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

depositing a layer of amorphous silicon which is between 10 and 5000 nanometers thick by sputtering or by plasma enhanced chemical vapor deposition hereafter referred to as PECVD using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals and/or gases which will not chemically attack or otherwise damage said substrate;

if higher mobilities or higher ON currents or lower threshold voltages for MOS transistors are needed for the transistors to be formed in said silcon layer than can be achieved in amorphous silicon, crystallizing said silicon layer to polycrystalline or microcrystalline form by pulse annealing the silcon layer with an excimer laser having a 308 nm wavelength using pulse durations of 30 nanoseconds or less full width at half maximum and energy density between 30-600 mJ/cm^2 per pulse using one or more pulses;

masking off areas of said integrated circuit where EEPROM cells, if any, are to be formed, and depositing a layer of gate insulator by PECVD at a

temperature below the glass transistion temperature of said substrate, said layer having a thickness suitable for thin film metal-oxide-semiconductor transistor device operation, typically between 20-500 nanometers thick;

masking off areas where MOS transistors are being formed to expose areas where EEPROM memory cells are to be formed and depositing one or more layers of gate insulator to form an insulation layer that is to lie below the floating gate, the thickness and materials selected for said one or more layers of gate insulator being such as to achieve Fowler-Noordheim tunnelling to the floating gate from a channel region at whatever programming voltage can be achieved on said integrated circuit, said deposition being accomplished by PECVD at a temperature below the glass transition temperature of said substrate;

depositing a layer of gate conductor, typically metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process to form a control gate at the MOS transistor locations and a floating gate at the EEPROM cell locations, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where EEPROM cells are being formed, and depositing a layer of intergate insulator from which will be formed the insulation layer between the floating gate and the control gate of each EEPROM cell, said deposition being accomplished by PECVD or some other process which will form an insulator of high enough quality to prevent charge leakage from said floating gate and at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where EEPROM cells are being formed, and depositing a layer of metal or silicide from which the control gate of all EEPROM cells is to be formed, said deposition being by PVD, CVD, PECVD, evaporation or

sputtering or some other suitable process and accomplished at a temperature below the glass transition temperature of said substrate;

performing the necessary photolithographic etching to define the gate islands at both said MOS transistor and EEPROM cell locations, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

doping the source and drain regions of all said MOS transistors and EEPROM cells using the Gas Immersion Laser Doping process or any other suitable doping process which can dope said source and drain regions to suitable conductivity and which crystallizes said amorphous silicon by pulsed laser annealing and which can be accomplished at a temperature below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

photolithographically etching to define the lateral extents of each thin film transistor island at each MOS transistor and EEPROM cell, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

depositing an insulation layer over all MOS transistors and EEPROM cells and etching vias therethrough for control gate contacts at all MOS transistor and EEPROM cell locations, said deposition being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing a layer of contact metallization conductor to fill said via holes and cover each MOS transistors and EEPROM cell location and the spaces therebetween, and photolithographically etching the conductor layer to form a contact metallization to connect all the control gates of all MOS transistors and EEPROM cells to other nodes in the circuit to form the rest of the connections necessary to form a desired integrated circuit functionality.

16. A process for manufacturing an integrated circuit with MOS and ROM cells formed over an antenna on a substrate comprising:

selecting a glass substrate having a large size which is compatible with the substrate size capacity of flat panel display manufacturing machines to be used to do the subsequent deposition, photolithography, etching and laser crystallization and annealing steps necessary to form said integrated circuit thereon;

using flat panel display manufacturing machines to perform the following steps:

depositing a layer of insulating material which has a thickness and Young's Modulus which are selected in light of the thickness and Young's Modulus of said substrate so as to reduce differential strain at anticipated operating temperatures so as to eliminate or reduce reliability problems using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals which will not chemically attack or otherwise damage said substrate;

forming an antenna with one or more terminals on said layer of insulating material deposited in the previous step at a plurality of locations on said substrate by any prior art process such as silk screening or deposition and photolithographic etching accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases that will not attack or otherwise damage said substrate;

using flat panel display manufacturing machines to perform the following steps:

depositing a layer of pad contact conductor such as metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process and photolithographically etching to form lead line conductors from each antenna terminal to the locations where RF input/output terminals of

each corresponding integrated circuit will be formed, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

depositing a layer of insulator over all MOS transistor and ROM cell locations and etching to form vias through said insulation layer where source and drain contacts are to be formed, said deposition being accomplished by PECVD or some other process which will form an insulator of high enough quality and at a temperature below the glass transition temperature of said substrate using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing a layer of contact metallization conductor such as metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process and photolithographically etching to form lead line conductors to make all necessary source and drain connections from each MOS transistor or ROM cell to other devices needed to establish at least part of the connections needed for the functionality of the integrated circuit being formed, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

depositing a layer of amorphous silicon which is between 10 and 5000 nanometers thick by sputtering or by plasma enhanced chemical vapor deposition hereafter referred to as PECVD using processing steps performed at temperatures or in a manner which will not exceed the glass transition temperature of said substrate and using chemicals and/or gases which will not chemically attack or otherwise damage said substrate;

if higher mobilities or higher ON currents or lower threshold voltages for MOS transistors are needed for the transistors to be formed in said silcon layer than can be achieved in amorphous silicon, crystallizing said silicon layer to polycrystalline or microcrystalline form by pulse annealing the silcon layer with an excimer laser having a 308 nm wavelength using

pulse durations of 30 nanoseconds or less full width at half maximum and energy density between 30-600 mJ/cm^2 per pulse using one or more pulses;

masking off areas of said integrated circuit where ROM cells, if any, are to be formed, and depositing a layer of gate insulator by PECVD at a temperature below the glass transistion temperature of said substrate, said layer having a thickness suitable for thin film metal-oxide-semiconductor transistor device operation, typically between 20-500 nanometers thick;

masking off areas where MOS transistors are being formed to expose areas where ROM memory cells are to be formed and depositing one or more layers of gate insulator to form an insulation layer that is to lie below the floating gate, the thickness and materials selected for said one or more layers of gate insulator being such as to achieve Fowler-Noordheim tunnelling to the floating gate from a channel region at whatever programming voltage can be achieved on said integrated circuit, said deposition being accomplished by PECVD at a temperature below the glass transition temperature of said substrate;

depositing a layer of gate conductor, typically metal or silicides by physical vapor deposition (hereafter PVD), chemical vapor deposition (hereafter CVD), PECVD, evaporation or sputtering or some other suitable process to form a control gate at the MOS transistor locations and a floating gate at the ROM cell locations, said deposition being accomplished at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where ROM cells are being formed, and depositing a layer of intergate insulator from which will be formed the insulation layer between the floating gate and the control gate of each ROM cell, said deposition being accomplished by PECVD or some other process which will form an insulator of high enough quality to prevent charge leakage from said floating gate and at a temperature below the glass transition temperature of said substrate;

masking off locations where MOS transistors are being formed to leave exposed only locations where ROM cells are being formed, and depositing a layer of metal or silicide from which the control gate of all ROM cells is to be formed, said deposition being by PVD, CVD, PECVD, evaporation or sputtering or some other suitable process and accomplished at a temperature below the glass transition temperature of said substrate;

performing the necessary photolithographic etching to define the gate islands at both said MOS transistor and ROM cell locations, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

doping the source and drain regions of all said MOS transistors and ROM cells using the Gas Immersion Laser Doping process or any other suitable doping process which can dope said source and drain regions to suitable conductivity and which crystallizes said amorphous silicon by pulsed laser annealing and which can be accomplished at a temperature below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

photolithographically etching to define the lateral extents of each thin film transistor island at each MOS transistor and ROM cell, said photolithographic etching being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attach or otherwise damage said substrate;

depositing an insulation layer over all MOS transistors and ROM cells and etching vias therethrough for control gate contacts at all MOS transistor and ROM cell locations, said deposition being accomplished at temperatures below the glass transition temperature of said substrate and using chemicals and/or gases which will not attack or otherwise damage said substrate;

depositing a layer of contact metallization conductor to fill said via holes and cover each MOS transistors and ROM cell location and the spaces therebetween, and photolithographically etching the conductor layer to form a

contact metallization to connect all the control gates of all MOS transistors and ROM cells to other nodes in the circuit to form the rest of the connections necessary to form a desired integrated circuit functionality.